

23. The semiconductor device according to claim 21 wherein said wiring is located below the surface smoothing film.

REMARKS

At the outset, the Examiner is thanked for the review and consideration of the present application. Additionally, the Examiner is thanked for indicating the allowance of claims 6-8 and 10.

The Examiner's Office Action dated August 9, 2001, has been received and its contents reviewed. Claims 1-12 were pending in the present application. By this Amendment, claims 13-23 have been added. Accordingly, claims 1-23 are pending, of which claims 1, 6, 9, 10, 11, 12, 13, 16, and 20 are independent.

Referring now to the Office Action, claims 9 and 11 are rejected under 35 U.S.C. § 112, second paragraph, as indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. More particularly, the feature "said voltage supply line" in the claims, as shown in line 5 of pages 45 and 47 of the specification, lacks proper antecedent basis. Applicant has amended claims 9 and 11, as shown above, to provide proper antecedent basis. Accordingly, the § 112, second paragraph, rejection is respectfully requested to be reconsidered and withdrawn.

Claims 1-5 are rejected under 35 U.S.C. § 103(a) as unpatentable over Tsjikawa et al. (U.S. Patent No. 5,951,570) in view of Hamada et al. (EP 0 414 478 A1).

Applicant respectfully submits that claim 12 was not addressed in the detailed Office Action.

The Examiner cited that Tsjikawa et al. discloses "an insulating film 141 or 200 nm thick insulating film (as in claim 2) formed over said substrate, said insulating film including at least first and second gate insulating films 134, 135 formed over the first and second conductor islands." However, Applicant respectfully submits that the insulating film 141 of Tsjikawa et al. is located below the semiconductor island and does not include the gate insulating films 134 and 135, as shown in Fig. 9B of Tsjikawa et al. Therefore, the Tsukukawa et al. is deficient in teaching, disclosing, or suggesting an insulating film formed over the substrate, wherein the

insulating film includes at least first and second gate insulating film formed over the first and second semiconductor islands, respectively.

Applicant respectfully submits that the presently claimed invention, as recited in the pending independent claims, further recite, among other features, "a wiring **formed on said insulating film** for electrically connecting one of the impurity regions of the first semiconductor island with the second gate electrode."

The Examiner asserted that it would have been obvious to connect one of the impurity regions on the first semiconductor island with the second gate electrode through the wiring 118 of Tsujikawa et al. in view of Hamada et al. However, Applicant respectfully submits that the Examiner has failed to address the feature in which the wiring is formed on the insulating film which includes the first and second gate insulating films.

It is well-established that, in order to show obviousness, all limitations in the claim must be taught or suggested by the prior art. In Re Boyka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974); MPEP § 2143.03. It is error to ignore specific limitations distinguishing over the references. In Re Boe, 184 U.S.P.Q. 38, 505 F.2d 1297 (C.C.P.A. 1974); In Re Saether, 181 U.S.P.Q. 36, 492 F.2d 849 (C.C.P.A. 1974); In Re Glass, 176 U.S.P.Q. 489, 472 F.2d 1388 (C.C.P.A. 1973). Applicant respectfully submits that a prima facie case of obviousness has not been established, as Tsujikawa et al. and Hamada et al. fail to teach, disclose, or suggest an insulating film formed over the substrate, wherein the insulating film includes at least first and second gate insulating film formed over the first and second semiconductor islands, respectively, and as the Examiner failed to address the claimed feature in which the wiring is formed on the insulating film which includes the first and second gate insulating films recited in the pending claims.

In view of the foregoing amendments and arguments, Applicant respectfully requests reconsideration and withdrawal of the U.S.C. § 103(a) rejections of claims 1-5, 9, 11, and 12.

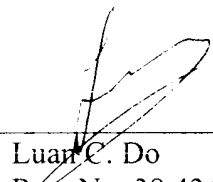
Newly added claims 13-23 recite that the first semiconductor island is a part of an NTFT while the second semiconductor island is a part of a PTFT. This feature is supported at least by the embodiment related to Fig. 7A of the present specification.

Applicant respectfully notes that new independent claims 13, 16, and 20 do not require that the wiring is formed on the insulating film which includes the first and second gate insulating films.

CONCLUSION

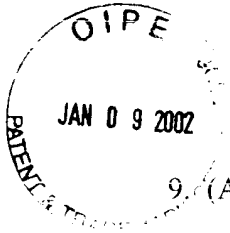
Having responded to all rejections set forth in the outstanding non-Final Office Action, it is submitted that claims 1-5, 9, 11, and 12 and new claims 13-23 are now in condition for allowance, as well as claims 6-8 and 10.. An early and favorable Notice of Allowance is respectfully solicited. In the event that the Examiner is of the opinion that a brief telephone or personal interview will facilitate allowance of one or more of the above claims, the Examiner is courteously requested to contact Applicant's undersigned representative.

Respectfully submitted,

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**VERSION OF AMENDED CLAIMS WITH
MARKINGS TO SHOW CHANGES MADE**

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9. (Amended) A semiconductor device comprising:
- a substrate having an insulating surface;
 - at least first and second semiconductor islands formed over said substrate wherein each of the semiconductor islands has a channel region and a pair of impurity regions;
 - an insulating film formed over said substrate, said insulating film including at least first and second gate insulating films formed over said first and second semiconductor islands, respectively;
 - at least first and second gate electrodes formed over said first and second semiconductor islands respectively with said first and second gate insulating films interposed therebetween;
 - a wiring formed on said insulating film for electrically connecting one of the impurity regions of the first semiconductor island with the second gate electrode wherein said wiring is connected to said one of the impurity regions through a hole opened in said insulating film;
 - a data line formed on said insulating film connected to the other one of the impurity regions of the first semiconductor island;
 - a first interlayer insulating film formed over the first and second semiconductor islands, the first and second gate electrodes, the wiring and the data line;
 - a voltage supply line formed on said first interlayer insulating film connected to one of the pair of impurity regions of the second semiconductor island;
 - an address line formed on said first interlayer insulating film connected to the first gate electrode wherein said address line extends across said data line;
 - a second interlayer insulating film formed over said first interlayer insulating film and said voltage supply line;
 - a pixel electrode formed over said second interlayer insulating film connected to the other one of the pair of the impurity regions of the second semiconductor island.

11. (Amended) A semiconductor device comprising:

a substrate having an insulating surface;

at least first and second semiconductor islands formed over said substrate wherein each of the semiconductor islands has a channel region and a pair of impurity regions;

an insulating film formed over said substrate, said insulating film including at least first and second gate insulating films formed over said first and second semiconductor islands, respectively;

at least first and second gate electrodes formed over said first and second semiconductor islands respectively with said first and second gate insulating films interposed therebetween;

a wiring formed on said insulating film for electrically connecting one of the impurity regions of the first semiconductor island with the second gate electrode wherein said wiring is connected to said one of the impurity regions through a hole opened in said insulating film;

a data line formed on said insulating film connected to the other one of the impurity regions of the first semiconductor island;

a first interlayer insulating film formed over the first and second semiconductor islands, the first and second gate electrodes, the wiring and the data line;

an address line formed on said first interlayer insulating film connected to the first gate electrode wherein said address line extends across said data line;

a surface smoothing film formed over said first interlayer insulating film and said [voltage supply] address line;

a pixel electrode formed over said [second interlayer insulating] surface smoothing film connected to the other one of the pair of the impurity regions of the second semiconductor island.